

# Pujitha A Weerakoon

pujitha.weerakoon@yale.edu

<http://www.med.yale.edu/cmphysiol/sigworth/people.html#pujitha>

U.S. permanent resident, authorized to work for any employer

## SUMMARY OF QUALIFICATIONS

An electrical/biomedical engineer with six years of mixed-mode integrated circuit design experience including transistor-level design, layout, silicon-chip testing and system integration. Successfully designed, fabricated and tested the first three VLSI prototypes of a high-bandwidth, low-noise, low-power, current-measuring biosensor fabricated in silicon-on-sapphire SOI technology, now being developed as a commercial product

## EDUCATION

- Ph.D., Engineering and Applied Science, Yale University, CT 2009
- M.Phil., M.S., Engineering and Applied Science, Yale University, CT 2006, 2007
- B.S.E., Electrical and Computer Engineering (Hons), Lafayette College, PA 2004

## RESEARCH AND WORK EXPERIENCE

- **Postdoctoral Research Associate**, Yale University, New Haven, CT (May 2009 – present)
  - Designing a commercial high-throughput integrated patch-clamp amplifier (PCA) biosensor system that records nanoampere ion-channel currents from 384 live cells in parallel.
  - The system consists of multi-channel, mixed-signal PCA ICs featuring rail-to-rail constant-transconductance operational amplifiers, current-to-voltage converters, active filters, digital-to-analog converters, and digital control circuitry.
  - Responsible for the entire IC design cycle and for its integration into a custom-built, high-throughput data acquisition system. Target customers are pharmaceutical companies that require high-throughput patch clamping to test medicines.
- **Engineering Consultant**, Warner Instrument Corp., Hamden, CT (May 2009 – present)
  - Leading the Yale-Warner collaboration to design a commercial high-throughput patch-clamp system.
- **Graduate Student**, Departments of Electrical and Biomedical Engineering, Yale University, New Haven, CT (September 2004 – May 2009)  
PIs: Drs. Frederick J. Sigworth and Eugenio Culurciello
  - Designed and fabricated a fully integrated, multi-channel, whole-cell patch-clamp amplifier system. Three generations of CMOS patch-clamp amplifier IC chips were fabricated; two in silicon-on-sapphire (SOS) CMOS technology and one in bulk CMOS technology. Responsible for the entire product development cycle including transistor-level circuit design and layout, PCB demo-board design, hands-on silicon-chip testing using live cells, and GUI based demo-system development.

- Designed, fabricated and tested a rail-to-rail, 75 dB, 12 MHz constant-transconductance operational amplifier in SOS CMOS for the patch-clamp system. This operational amplifier is the first rail-to-rail, constant-transconductance amplifier made in SOS.
  - Proposed and implemented a novel solution to fully compensate the resistance of the recording electrode of patch-clamp amplifiers to increase accuracy and bandwidth by integrating a phase-lag controller to the system.
- **Research Assistant**, Department of Electrical and Computer Engineering, Lafayette College, Easton, PA (September 2002 – May 2004)
    - Electrically modeled the human cardiovascular system connected to a rotary ventricular assist device (VAD) using Matlab and Simulink.
    - Proposed a novel index for minimally invasive estimation of cardiac function for patients with rotary VAD support.

## AREAS OF EXPERTISE

- **Mixed-Mode Custom VLSI Systems:** Experienced in full-custom analog/mixed-signal design, fabrication and testing. Experienced with low-noise IC circuit design and noise reduction techniques. Expertise in designing, fabricating and testing analog building blocks such as operational amplifiers, digital-to-analog converters (DACs), analog-to-digital converters (ADCs), comparators, and filters
- **Electronic Design and Automation Tools:** Experienced with Cadence custom IC EDA design tools, Orcad PCB design tools, Modelsim, Xilinx ISE. Experienced on Linux/Solaris systems.
- **Integrated Circuit Testing and Modeling:** Experienced with PCB design for IC characterization. Proficient in designing embedded-system testbeds for IC testing using field programmable gate arrays (FPGAs) and graphical-user interfaces (GUIs). Experienced modeler in Matlab and Simulink.
- **Programming Languages:** Experienced programmer in C/C++, Java, VHDL and Verilog.

## AWARDS AND HONORS

- Lafayette College scholarship for undergraduate studies (September 2000 – May 2004)
- Lafayette College's Jeffery. B. Havens award for research (Year 2003)
- Inducted into the Eta Kappa Nu national electrical engineering honor society (Year 2003)
- Inducted into the Pi Mu Epsilon national mathematic honor society (Year 2002)

## **PUBLICATIONS**

### **Peer Reviewed**

1. P. Weerakoon, Eugenio Culurciello, K. Klemic, F. J. Sigworth, "An Integrated Patch-Clamp Potentiostat with Electrode Compensation", IEEE Transactions on Biomedical Circuits and Systems TBCAS, April 2009, Vol. 3, Issue 2, pp. 117-125 (invited paper).
2. P. Weerakoon, K. Klemic, F. J. Sigworth, E. Culurciello, "An Integrated Patch-Clamp Amplifier for High-Throughput Planar Patch-Clamp Systems", IEEE International Symposium on Circuits and Systems, 2008. ISCAS 2008, May 2008, Seattle, pp. 1808-1811.
3. P. Weerakoon, K. Klemic, F. J. Sigworth, E. Culurciello, "An Integrated Patch-Clamp Biosensor for High-Density Screening of Cell Conductance", IET Electronics Letters, June 2008, Volume 44, Issue 2, pp. 81-82.
4. P. Weerakoon, K. Klemic, F. J. Sigworth, E. Culurciello, "A Low-Noise Miniaturized Patch-Clamp Amplifier", IEEE LISA 2007 conference proceedings, NIH November 8<sup>th</sup> 2007.
5. P. Weerakoon, K. Klemic, F. J. Sigworth, E. Culurciello, "Electrical Noise Analysis of an Integrated Patch-Clamp Amplifier", IEEE BioCAS 2007 conference proceedings, Montreal November 28<sup>th</sup> 2007.
6. P. Weerakoon, K. Klemic, F. J. Sigworth, E. Culurciello, "An Integrated Patch-Clamp Amplifier for High-Density Whole-Cell Recordings", IEEE International Symposium on Circuits and Systems, 2007. ISCAS 2007, 27-30 May 2007, pp. 1205-1209.
7. P. Weerakoon and E. Culurciello, "Three-Dimensional Photodetectors in 3D Silicon-on-Insulator Technology", IEE Electron Device Letters, Vol. 28, Issue 2, February 2007, pp 117-119.
8. Z. Fu, P. Weerakoon, E. Culurciello, "A Nano-Watt Silicon-on-Sapphire ADC using 2C-1C Capacitor Chain", Electronic Letters, Volume 42, Issue6, 2006.
9. P. Weerakoon and Y. Yu, "Minimally Invasive Estimation of Cardiac Function for Patients with Rotary VAD Support." American Control Conference, June 8-10, 2005, Portland, pp. 3812-3816.
10. P. Weerakoon and Y. Yu, "Sensitivity Analysis of Cardiac Function Detection for Patients with Ventricular Assist Device Support", Proceedings of the IEEE 30th Annual Northeast Bioengineering Conference, 2003, Springfield, MA.
11. P. Weerakoon and I. Jouny, "An Email Retrieval System Through a Phone Line", Proceedings of IEEE ICME, 2003, Baltimore, MD.

### **In Preparation**

1. P. Weerakoon, F. J. Sigworth, P. J. Kindlmann, E. Culurciello, "A 75dB 12MHz Operational Amplifier in Silicon-on-Sapphire with Constant Transconductance", *Submitted*, 2009.
2. P. Weerakoon, E. Culurciello, Y. Yang, J. Santos-Sacchi, P. J. Kindlmann, F. J. Sigworth, "A Two-Channel Patch-Clamp System on a Chip for Automatic High-Throughput Whole-Cell Recording Systems", *Submitted*, 2009.

## **PROFESSIONAL AFFILIATIONS AND EXPERIENCES**

- IEEE member
- Invited reviewer for IEEE transactions on circuits and systems, IEEE transactions on biomedical circuits and systems